AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Previously Presented) The successive approximation ADC system of claim 24, further comprising logic operative to adjust the successive approximation value based on the digital signal.

3. (Previously Presented) The successive approximation ADC system of claim 2, wherein the multi-bit analog to digital converter has a range, the logic being responsive to adjust the successive approximation value based on the digital signal to place the digital signal within the range of the multi-bit analog to digital converter.

4. (Previously Presented) The successive approximation ADC system of claim 3, wherein the logic appends the digital signal to the successive approximation value to increase the resolution of the successive approximation value after the digital signal is within the range of the multi-bit analog to digital converter.

5. (Previously Presented) The successive approximation ADC system of claim 3, wherein the logic calibrates the digital signal in accordance with the successive approximation value after the digital signal is within the range of the multi-bit analog to digital converter.

6. (Previously Presented) The successive approximation ADC system of claim 3, the logic being operative to adjust the successive approximation value based on the digital signal by performing a single bit iteration when the amplified signal is outside the range of the multi-bit analog to digital converter, starting with most significant bit first to least significant bit, until the amplified signal is within the range of the multi-bit analog to digital converter.

7. (Previously Presented) The successive approximation ADC system of claim 6, the logic being operative to append a value of the digital signal to the least significant bits of the successive approximation value after the amplified signal is within range of the multi-bit analog to digital converter.

8. (Previously Presented) The successive approximation ADC system of claim 7, the logic calibrating the digital signal according to the successive approximation value.

9. (Previously Presented) The successive approximation ADC system of claim 3, further comprising

a clock source to produce clock signals;

a signal generating circuit to generate and output a repetitive test waveform to a device under test in accordance with the clock signals, the device under test outputting the test signal; and

a pulse generating circuit coupled to the clock circuit for producing sampling point signals corresponding to sampling points spaced across the test signal based on the clock signals;

the multi-bit analog to digital converter being operative to convert the amplified signal to the digital signal based on the sampling point signals resulting in a digitized waveform corresponding to the test signal.

10. (Previously Presented) The successive approximation ADC system of claim 9, wherein the sampling point signals sample the test signal at a sample rate less than the Nyquist rate of the test signal.

11. (Previously Presented) The successive approximation ADC system of claim 9, further comprising a second clock source producing a second clock signal, the pulse generating circuit being operative to determine a frequency ratio between the clock source and the second clock source and to employ the frequency ratio for producing the sampling point signals.

12. (Previously Presented) The successive approximation ADC system of claim 11, wherein the frequency ratio is selected to minimize time, resulting in a scrambled sample order, the successive approximation system further comprising a descrambling system to reorder the samples before outputting the digitized waveform.

13. (Currently Amended) The successive approximation ADC system of claim 6, wherein at least one of the pulse generating circuit, memory, clock circuit, and signal generating circuit are implemented on the same integrated circuit as the circuit under test and the comparison system.

14. (Previously Presented) A coherent undersampling digitizer, comprising:

means for receiving a repetitive test signal from a device under test in accordance with first clock signals;

means for producing a difference signal based on the difference between the repetitive test signal and a successive approximation signal;

means for amplifying the difference signal; and

means for converting the amplified difference signal to a multi-bit digital comparison signal wherein the converting means operates as a comparator until the amplified difference signal is within range of the converting means.

15. (Original) The coherent undersampling digitizer of claim 14, the means for converting producing a first signal when the amplified difference signal is outside a range of the means for converting, and producing a second signal indicative of magnitude of the amplified difference signal when the amplified difference signal is within the range of the means for converting.

16. (Original) The coherent undersampling digitizer of claim 14, the means for producing sampling point signals being responsive to a ratio between the first clock signals and second clock signals and to generate the successive approximation signal based on the multi-bit digital comparison signal.

17. (Previously Presented) The coherent undersampling digitizer of claim 15, the means for producing sampling point signals generating single bit iterations of the successive approximation signal while the first signal is produced and a multi-bit iteration of the successive approximation signal when the second signal is produced.

18. (Currently Amended) A method for successive approximation undersampling analog to digital conversion, comprising:

combining a test signal with a successive approximation signal;

amplifying the combined signal to generate an amplified combined signal;

converting the amplified combined signal to a multi-bit digital comparison signal using a multibit analog to digital converter that operates as a comparator until the amplified combined signal is within range of the analog to digital converter; and

adjusting the successive approximation signal based on the digital comparison signal.

19. (Cancelled)

20. (Previously Presented) The method for successive approximation analog to digital conversion of claim 18, further comprising decreasing the successive approximation value by one bit when the digital comparison signal is at a minimum value.

21. (Previously Presented) The method for successive approximation analog to digital conversion of claim 18, further comprising increasing the successive approximation value by one bit when the digital comparison signal is at a maximum value.

22. (Previously Presented) The method for successive approximation analog to digital conversion of claim 18, further comprising combining the successive approximation signal with the digital comparison signal when the digital comparison signal is within a predetermined range of circuitry that performs the converting.

23. (Previously Presented) The method for successive approximation analog to digital conversion of claim 22, further comprising calibrating the digital comparison signal to a scale corresponding to a scale of the successive approximation signal.

24. (Currently Amended) A ~~Successive~~ successive approximation undersampling ADC system comprising:

a memory having a successive approximation value;

a summer coupled to a test signal and an output of the memory to generate a difference signal being a difference therebetween;

an amplifier coupled to an output of the summer to generate an amplified signal from the difference signal;

a single multi-bit analog to digital converter coupled to an output of the amplifier to convert the amplified signal to a digital signal wherein the analog to digital converter operates as a comparator until the amplified signal is within range of the analog to digital converter.